REMARKS

The following remarks are made in response to the Office Action mailed June 16, 2006. Claims 1-29 were rejected. With this Response, claim 2 has been cancelled without prejudice, and claims 1, 3-5, 12, 21, and 26 have been amended. Claims 1 and 3-29 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-2, 5-15, 19, 22-26, and 29 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,036,068 to Davis et al. ("Davis Patent").

Claims 3, 16, and 27-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Davis Patent as applied to claims 1-2, 5-15, 19, 22-26 and 29 above, and further in view of U.S. Patent No. 5,428,630 to Weng et al. ("Weng Patent").

Claims 4 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Davis Patent as applied to claims 1-2, 5-15, 19, 22-26 and 29 above, and further in view of U.S. Patent No. 6,738,942 to Sridharan et al. ("Sridharan Patent").

Amended independent claim 1 recites a memory including an array of memory cells and a control circuit, wherein the control circuit is configured to read error correction coded data from the array of memory cells, to evaluate an integrity of the error correction coded data and select error correction coded data having compromised integrity, and to provide error correction code decoding to only the selected error correction coded data and to discard unused error correction code parity data of unselected error correction coded data.

The Davis Patent does not teach or suggest the invention as recited by amended independent claim 1. The Davis Patent describes a magnetoresistive solid state storage device 1 comprising an array 10 of storage cells 16 coupled to a controller 20 including an ECC coding and decoding unit 22 (see Figure 1 and col. 1, lines 42-46). With reference to Figure 3, the Davis Patent describes a method of recovering error correction encoded data from a solid state storage device, such as solid state storage device 1. The method includes a step 301 of accessing a plurality of storage cells 16 to read a block of data stored therein, a step 302 of obtaining parametric values, such as a resistance, of each accessed storage cell 16, steps 303 and 304 of generating erasure information based on the parametric values from step 302, a step 305 of error correction decoding the block of data using an ECC scheme and the

erasure information generated at 305, and providing an output at 306 as recovered information from the error correction decoding of step 305.

The method described by the Davis Patent provides error correction decoding for each block of data read from array 10 of storage cells 16 and employs the erasure information generated from the parametric values to improve the error correction capability of the ECC scheme employed by ECC coding and decoding unit 22. In one example, the ECC scheme is a [160, 128, 33] Reed-Solomon code. Normally, such a Reed-Solomon code, producing codewords having one-hundred-sixty 8-bit symbols corresponded to 128-bytes of original information and a minimum distance of thirty-three symbols is able to locate and correct up to sixteen symbol errors (see Col. 6, lines 25-36). By employing the erasure information generated from the parametric values, such a Reed-Solomon code is mathematically able to correct up to sixteen full errors or up to thirty-two erasures (or a combination such as twenty erasures and six full errors, thereby increasing the number of errors able to be corrected (see Col. 8, lines 53-67).

In light of the above, the Davis Patent does not teach or suggest a memory including **a control circuit configured to read error correction coded data from the array of memory cells, to evaluate an integrity of the error correction coded data and select error correction coded data having compromised integrity, and to provide error correction code decoding to only the selected error correction coded data and to discard unused error correction code parity data of unselected error correction coded data,** as recited by amended independent claim 1. The Davis Patent describes using an ECC scheme, such as a Reed-Solomon scheme or other suitable scheme (e.g. BCH) (see Col. 5, lines 52-62), to ECC decode every block of data read from array 10 of storage cells 16 and employs erasure information associated with storage cells 16 to increase the number of errors that can be located and corrected by the ECC scheme. The Davis Patent does not teach or suggest evaluating an integrity of the error correction coded data and providing error correction decoding to only error correction coded data having compromised integrity. As such, the Davis Patent does not teach or suggest the present invention as recited by amended independent claim 1.

Amended independent claim 12 recites a magnetic memory including a macro-array of memory cells and a control circuit, wherein the control circuit is configured to read the

macro-array of memory cells to obtain ECC encoded data comprising ECC parity data, to evaluate the ECC encoded data reliability while leaving the ECC parity data idle, and to provide error correction decoding to only the ECC encoded data deemed unreliable based on the reliability evaluation. Amended independent claim 12 includes limitations similar to those recited by independent claim 1. As such, for reasons similar to those described above with respect to independent claim 1, the Davis Patent does not teach or suggest the present invention as recited by amended independent claim 12.

Amended independent claim 21 recites a magnetic memory including means for storing data encoded with an ECC scheme, means for reading the ECC encoded data, means for identifying corrupted ECC encoded data, means for decoding only ECC encoded data identified as corrupted. Amended independent claim 21 includes limitations similar to those recited by independent claim 1. As such, for reasons similar to those described above with respect to independent claim 1, neither the Davis Patent nor the Sridharan Patent, either alone or in combination, teach or suggest the present invention as recited by independent claim 21.

Amended independent claim 26 recites a method for writing to and reading from a magnetic memory, the method including reading ECC encoded data from the memory, evaluating non-ECC parity data to obtain an evaluation result; and decoding the ECC encoded data to obtain recovered data only if the evaluation result indicates the ECC encoded data is corrupted. Amended independent claim 26 includes limitations similar to those recited by independent claim 1. As such, for reasons similar to those described above with respect to independent claim 1, the Davis Patent does not teach or suggest the present invention as recited by amended independent claim 26.

In view of the above, Applicants respectfully request that the rejection of independent claims 1, 12, 21, and 26 under 35 U.S.C. § 103(a) be withdrawn and that these claims be allowed. Furthermore, dependent claims 3-11 further define patentably distinct independent claim 1, dependent claims 13-20 further define patentably distinct independent claim 12, dependent claims 22-25 further define patentably distinct independent claim 21, and dependent claims 27-29 further define patentably distinct independent claim 26. As such, Applicants respectfully request that the rejection of dependent claims 3-11, 13-20, 22-25, and 27-29 under 35 U.S.C. § 103(a) be withdrawn and that these claims be allowed as well.

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CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1 and 3-29 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1 and 3-29 is respectfully requested.

Amendment and Response
Applicant: Todd Christopher Adelmann
Serial No.: 10/659,630
Filed: September 10, 2003
Docket No.: 200208961-1
Title: MAGNETIC MEMORY WITH ERROR CORRECTION CODING

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005 or N. Rhys Merrett at Telephone No. (425) 402-4638, Facsimile No. (425) 489-9594. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 13 day of September, 2006.

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